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PTO/SB/05 (2/98)

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for nonprovisional applications under 37 CFR § 1.53(b))

Attorney Docket No.	660073.488D1
First Inventor or Application Identifier	Pierre C. Fazan
Title	METHOD AND APPARATUS FOR TRENCH ISOLATION PROCESS WITH PAD GATE AND TRENCH EDGE SPACER ELIMINATION
Express Mail Label No.	EL251277725US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Box Patent Application, Assistant Commissioner for Patents, Washington, D.C. 20231

1. [X] General Authorization Form & Fee Transmittal *(Submit an original and a duplicate for fee processing)*
2. [X] Specification [Total Pages] 17 *(preferred arrangement set forth below)*
   - Descriptive Title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 USC 113)* [Total Sheets] 5
4. Oath or Declaration [Total Pages] 2
   a. [ ] Newly executed (original or copy)
   b. [X] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)
5. [X] Incorporation By Reference *(useable if box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer-Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [X] Preliminary Amendment
13. [X] Return Receipt Postcard
14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [X] Other: Certificate of Express Mail; Check

17. **If a CONTINUING APPLICATION,** *check appropriate box and supply the requisite information below and in a preliminary amendment*

[ ] Continuation [X] Divisional [ ] Continuation-In-Part (CIP) of prior Application No.: 09/032,231

Prior application information: Examiner **Mahshid Saadat** Group / Art Unit **2815**

[ ] Claims the benefit of Provisional Application No. _____

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Respectfully submitted,

TYPED or PRINTED NAME Frank Abramonte REGISTRATION NO. 38,066

SIGNATURE _____ Date August 31, 1999

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08/31/99 US PTO

09/386646 C510 U.S. PTO 08/31/99

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Present Application:

Applicants	:	Pierre C. Fazan and Gurtej S. Sandhu
Title	:	METHOD AND APPARATUS FOR TRENCH ISOLATION PROCESS WITH PAD GATE AND TRENCH EDGE SPACER ELIMINATION
Docket No.	:	660073.488D1
Date	:	August 31, 1999

Prior Application:

Examiner	:	Mahshid Saadat
Art Unit	:	2815
Application No.	:	09/032,231

Box Patent Application
Assistant Commissioner for Patents
Washington, DC 20231

PRELIMINARY AMENDMENT

Sir:

Please amend the above-identified application as follows:

In the Specification:

Amend the specification by inserting a new section before the "Technical Field" as follows:

-- CROSS-REFERENCE TO RELATED APPLICATION

This application is a divisional of pending United States Patent Application No. 09/032,231, filed February 27, 1998. --

<u>In the Claims</u>:

Please cancel claims 1-21.

REMARKS

Prior to substantive examination of the above divisional application, please cancel claims 1-21. Claims 22-34 are now pending in this application.

Respectfully submitted,

Pierre C. Fazan and Gurtej S. Sandhu

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METHOD AND APPARATUS FOR TRENCH ISOLATION PROCESS WITH PAD GATE AND TRENCH EDGE SPACER ELIMINATION

TECHNICAL FIELD

The present invention relates generally to trench isolation structures on microelectronic devices and methods for forming the same, and more specifically to oxide spacers which are formed about trench isolation structures.

BACKGROUND OF THE INVENTION

Microelectronic devices are used in computers, communications equipment, televisions and many other products. Typical microelectronic devices include processors, memory devices, field emission displays and other devices that have circuits with small, complex components. In current manufacturing processes, the components of such circuits are generally formed on a microelectronic substrate or wafer with conductive, insulative and semiconductive materials. Fifty to several hundred microelectronic devices are typically formed on each microelectronic substrate, and each microelectronic device may have several million components.

Because fabricating microelectronic devices generally involves forming electrical components at a number of layers and locations, microelectronic devices generally have many conductive features to couple the various components together.

The method by which the components of an integrated circuit are interconnected involves the fabrication of metal strips that run across an oxide layer in the regions between rows of transistors. However, the strips, together with the oxide beneath the strips, form gates of parasitic MOS transistors and diffused regions adjacent the strips form sources and drain regions, respectively, of the parasitic MOS transistors. The threshold voltage of such parasitic transistors must be kept higher than any possible operating voltage so that

spurious channels will not be inadvertently formed between the devices. In order to isolate MOS transistors, then, it is necessary to prevent the formation of channels in the field regions, implying that a large value of V_T is needed in the field regions.

Implementing electronic circuits involves connecting isolated devices through specific electrical paths. When fabricating silicon integrated circuits it must therefore be possible to isolate devices built into the silicon from one another. These devices can subsequently be interconnected to create the specific circuit configurations desired. Isolation technology is one of the most critical aspects of fabricating integrated circuits. Hence, a variety of techniques have been developed to isolate devices in integrated circuits. These techniques balance competing requirements, such as minimum isolation spacing, area of footprint, surface planarity, process complexity, and density of defects generated during fabrication of the isolation structure.

One of the most important techniques developed is termed LOCOS isolation (for LOCal Oxidation of Silicon), which involves the formation of a semi-recessed oxide in the nonactive (or field) areas of the substrate for use with PMOS and NMOS integrated circuits. Conventional LOCOS isolation technologies reach the limits of their effectiveness as device geometries reach submicron size. Modified LOCOS processes such as trench isolation have had to be developed to deal with these smaller geometries.

Refilled trench structures have been used as a replacement for conventional LOCOS isolation techniques. Trench/refill approaches for isolation applications generally fall into the following three categories: shallow trenches (less than 1 micron); moderate depth trenches (1-3 micron); and deep, narrow trenches (greater than 3 micron deep, less than 2 micron wide). Shallow, refilled trenches are used primarily for isolating devices of the same type, and hence they can be considered as replacements for LOCOS isolation. An example of a shallow trench isolation structure is shown in Figure 1.

The conventional shallow trench isolation structure 10 shown in Figure 1 is fabricated on a microelectronic substrate 20. Gate structures 100 and 300 are formed on the substrate 20 from a pad/gate oxide layer 30, a first gate layer 40, a second gate layer 70 and a silicide layer 80. A trench 22 formed in the substrate 20 is filled with a silicon oxide 60, to form the shallow trench isolation structure or isolation pad 400. An isolated component 200 is fabricated on the isolation pad 400, the isolated component 200 comprising the second gate layer 70 and the silicide layer 80. Oxide spacers 91 - 94 are then formed about the gate structures 100 and 300, the isolated component 200 and the isolation pad 400. The oxide spacers 91-94 protect the components from contact with other conductive components, as well as, providing gentle slopes to improve step coverage when applying additional layers. Generally, the less severe the slope, the better the coverage.

Due to the need to define gentle slopes from the relatively tall gate structures 100, 300, the isolated component 200, and the isolation pad 400, the spacers 91-94 take up a large amount of area on the microelectronic substrate 20. Continued progress in microelectronic fabrication requires that isolation structures be as small as possible and take up a minimum of area on the microelectronic substrate. Any reduction in the size of the isolation structures will provide great benefits in semiconductor manufacture.

SUMMARY OF THE INVENTION

A reduction in the size of isolation shallow trench structures and associated gates is achieved by the elimination of spacers about the isolation pad and the reduction in the area occupied by spacers around the associated gate structures and the isolation component. The elimination of the spacer around the isolation pad, and the reduction in size of the other spacers is achieved by controlling the height by which the isolation pad extends from the substrate.

In a first exemplary embodiment, the isolation pad is recessed to a level which is between an upper level of the first gate layer and an upper level of the substrate of the microelectronic substrate.

In a second embodiment, the height of the isolation pad is controlled relative to the height of the gate structure by ensuring that the gate structure is at least approximately twice the height of the height by which the isolation pad extends beyond the substrate. Likewise, spacer size can be controlled by ensuring that the isolation pad extends beyond the substrate by a height which is less than approximately one half of the height of the gate structure.

Controlling the relative heights of the isolation pad relative to the gate structures or the isolated component is accomplished by recessing the isolation pad during the fabrication process.

In one exemplary embodiment of the fabrication process, the gate oxide layer is grown on the microelectronic substrate. The first gate layer is deposited on the gate oxide layer and the trench is formed through the gate layer and the gate oxide layer and into the substrate. The trench is then filled with the silicon oxide, and the structure is planarized through chemical-mechanical planarization (CMP). The field oxide is then recessed to an appropriate depth. It is this recess step which controls the later spacer formation. After recessing, the second gate layer is deposited over the recessed field oxide and the first gate layer. The silicide layer is then formed over the second gate layer and gate structures and the isolated component are formed in the silicide layer, the first and second gate layers, and the gate oxide layer. Spacers are formed about the resulting gate structures and the isolated component.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-sectional view showing a conventional method for the fabrication of a shallow trench isolation structure having spacers.

Figures 2A-2H are cross-sectional views showing respective steps of a method for the fabrication of a shallow trench isolation structure in a microelectronic substrate, according to an exemplary embodiment of the present invention.

Figure 3 is a flow chart of the method steps in the exemplary embodiment of Figures 2A-2G.

DETAILED DESCRIPTION OF THE INVENTION

In the following description, certain specific details are set forth in order to provide a thorough understanding of various embodiments of the present invention. However, one skilled in the art will understand that the present invention may be practiced without these details. In other instances, well-known structures associated with microelectronic devices and with the fabrication of microelectronic devices, and isolation structures in microelectronic devices, have not been shown in detail in order to avoid unnecessarily obscuring the description of the embodiments of the invention.

With reference to Figures 2A and 3, a pad oxide or gate oxide layer 30 is formed on a surface 24 of a microelectronic substrate 20 in step 100. The gate oxide layer 30 has an exposed upper surface 32. The substrate 20 may be formed of glass or other suitable material, but is preferably formed of silicon. The gate oxide layer 30 may be formed by first cleaning a bare silicon surface of substrate 20 and then thermally growing a SiO_2 layer thereupon. Other techniques for forming the gate oxide layer 30 may be used, such as CVD SiO_2 deposition.

With reference to Figures 2B and 3, a first gate layer 40 is deposited over the gate oxide layer 30 in step 102. The first gate layer 40 has an upper surface 42. The first gate layer 40 preferably consists of polysilicon. A nitride stop layer 50 may optionally be formed over the first gate layer 40 in step 104. The stop layer 50 may be CVD silicon nitride which functions as an oxidation mask.

With reference to Figures 2C and 3, in steps 106 and 108, a trench 22 is formed, the trench 22 extending through the stop layer 50, the first gate layer 40, the gate oxide layer 30 and into the substrate 20. The trench 22 defines a field area 24 in the substrate 20. A thin layer (100-200Å) of silicon dioxide (SiO_2) is then thermally grown on the exposed silicon (Si).

With reference to Figures 2D and 3, the trench 22 is filled with silicon oxide to form a field oxide 60 in step 110. Silicon oxide can be deposited using conventional techniques such as LPCVD, HDPCVD (high density plasma CVD), etc. Conventional processes may be used to reduce or eliminate the birds beak which often results from field oxide growth. Chemical-mechanical planarization (CMP) is then used to planarize the field oxide 60 in step 112. In general, CMP involves holding or rotating a wafer of semiconductor material against a wetted polishing surface under controlled chemical slurry, pressure, and temperature conditions. A chemical slurry containing a polishing agent such as alumina or silica may be utilized as the abrasive medium. Additionally, the chemical slurry may contain chemical etchants. This procedure may be used to produce a surface with a desired endpoint or thickness, which also has a polished and planarized surface. If the optional stop layer 50 is formed, the stop layer 50 will normally determine the endpoint of the CMP step 112. The stop layer 50 is then removed in step 114 by conventional means.

With reference to Figures 2E and 3, the field oxide 60 is recessed in step 116 such that the surface of the field oxide 60 is at a level between the level of the upper surface 42 of the first gate layer 40 and the surface 24 of substrate 20. In the exemplary embodiment, the field oxide level is between the upper surface 42 of the first gate layer 40 and the upper surface 32 of the gate oxide layer 30.

With reference to Figures 2F and 3, a second gate layer 70 may be formed on the recessed field oxide 60 and the first gate layer 40 in step 118. The second gate layer 70 serves as an adhesion layer. The second gate layer 70 is

preferably composed of polysilicon. The second gate layer 70 can be formed by conventional deposition methods.

A conductive layer 80 is then formed over the second gate layer 70 in step 120. The conductive layer 80 may be formed by chemical vapor deposition of tungsten silicide (WSi_X). Other refracting metal silicides may be used, including, but not limited to $TiSi_2$, $TaSi_2$, $MoSi_2$, PtSi. A thin layer of oxide may optionally be formed on the silicide layer 80.

Gate structures 100, 300 are next formed in the silicide conductive layer 80, the first and second gate layers 40, 70 and the gate oxide layer 30 in step 122 as shown in Figure 2G. The shallow trench isolation structure 400 may also be uncovered at this point. The gates 100, 300 are formed through conventional patterning and etching processes. The isolated component 200 may also be formed at this point.

With reference to Figures 2H and 3, spacers 91 and 92 are formed about the gate structures 100 and 300, respectively, and spacer 92 is formed about the isolated component 200 in step 124. Formation of the spacers may be carried out in a number of ways including deposition of LPCVD-SiO_2. The spacers 91-93 are grown until an adequate reduction of step size is achieved. Due to the relatively low profile of the isolation pad 400, little or no spacer will form adjacent to the isolation pad 60. To achieve this, the field oxide isolation pad height 66 should be approximately one half of the height of the gate structure 106, 306, an approximately two-to-one ratio.

Although specific embodiments of the shallow trench isolation structure and method of the present invention have been described above for illustrative purposes, various equivalent modifications may be made without departing from the spirit and scope of the invention, as will be recognized by those skilled in the relevant art. The teachings provided herein of the present invention can be applied to other isolation structures, not necessarily the exemplary shallow trench isolation structure generally described above. For example, additional layers may be formed or the order of forming layers may be

changed. The substrate may be composed of silicon, glass or some combination of other materials or layers of materials. Alternatively, different materials may be employed, and different methods of forming or depositing the layers may be used.

These and other changes can be made to the invention in light of the above detailed description. In general, in the following claims, the terms should not be construed to limit the invention to the specific embodiments disclosed in the specification claims, but should be construed to include all apparatus and methods for forming trench isolation structures with reduced and eliminated spacers. Accordingly, the invention is not limited by the disclosure, but instead its scope is to be determined entirely by the following claims.

CLAIMS

1. A method of forming a trench isolation structure comprising the steps of:

supplying a microelectronic substrate;

forming a trench in the microelectronic substrate;

depositing a field oxide in the trench, the field oxide projecting above the substrate to a height that is small enough to prevent the formation of spacers about the field oxide.

2. A method of forming a trench isolation structure on a microelectronic substrate, the method comprising the steps of:

forming a trench in the microelectronic substrate;

depositing a field oxide in the trench extending from the trench to a height which is less than half of a height of a gate structure to be formed on the substrate;

forming the gate structure on the substrate; and

forming a spacer adjacent the gate structure.

3. A method of forming a trench isolation structure on a microelectronic substrate, the method comprising the steps of:

depositing a field oxide isolation pad extending from a recess in the substrate to a field oxide isolation pad height;

forming a gate structure on the substrate having a height which is at least twice the height of the field oxide isolation pad height; and

forming a spacer adjacent the gate structure.

4. A method of forming a trench isolation structure on a microelectronic substrate, the method comprising the steps of:

forming a trench in the microelectronic substrate;

depositing a field oxide isolation pad extending from the trench by height which is less than half of a height of a component to be formed on the field oxide isolation pad;

forming the component on the field oxide isolation pad; and

forming a spacer adjacent the component.

5. A method of forming a trench isolation structure on a microelectronic substrate, the method comprising the steps of:

depositing a field oxide isolation pad extending from a recess in the substrate to a field oxide isolation pad height;

forming a component on the field isolation pad having a height which is at least twice the height of the field oxide isolation pad height; and

forming a spacer adjacent the component.

6. A method of forming a trench isolation structure on a microelectronic substrate, the method comprising the steps of:

growing a gate oxide layer on the microelectonic substrate;

depositing a first gate layer on the gate oxide layer;

forming a trench, the trench extending though the first gate layer, the gate oxide layer and into the substrate;

filing the trench with a field oxide;

planarizing the field oxide;

recessing the field oxide;

depositing a second gate layer over the recessed field oxide and the first gate layer;

forming a silicide layer over the second gate layer;

forming at least one gate structure in the silicide layer, the first and the second gate layers and the gate oxide layer; and

forming a spacer adjacent the gate structure.

7. The method of claim 6 wherein the step of recessing the field oxide includes the step of

recessing the field oxide to a depth that is below an upper surface of the first gate layer.

8. The method of claim 6 wherein the step of recessing the field oxide includes the step of

recessing the field oxide to a depth that is above an upper surface of the substrate.

9. The method of claim 6 wherein the step of recessing the field oxide includes the step of

recessing the field oxide to a depth that is between an upper level of the first gate layer and an upper level of the substrate.

10. The method of claim 6 wherein the step of recessing the field oxide includes the step of

recessing the field oxide to a depth that is below an upper level of the first gate layer and that is at least even with an upper level of the substrate.

11. The method of claim 6 wherein the step of recessing the field oxide includes the step of

recessing the field oxide to a level which extends beyond an upper level of the substrate by a height which is less than or equal to approximately one half of a height of the gate structure.

12. The method of claim 11, further comprising the step of

depositing a stop layer on the first gate layer before etching the trench.

13. The method of claim 12, wherein the step of forming a trench includes the step of

etching through the stop layer, the first gate layer, the gate oxide layer; and etching into the substrate.

14. The method of claim 13, further comprising the step of

removing the stop layer after planerizing the field oxide.

15. The method of claim 6 wherein the step of depositing a first gate layer includes the step of

depositing a layer of polysilicon on the gate oxide layer.

16. The method of claim 6 wherein the step of depositing a second gate layer includes the step of

depositing a layer of polysilicon on the recessed field oxide and the first gate layer.

17. The method of claim 6 wherein the step of forming a silicide layer includes the step of

depositing a layer of tungsten silicide on the second gate layer by chemical vapor disposition.

18. The method of claim 6, wherein the step of forming the silicide layer includes the step of:

depositing a conductor by chemical vapor disposition on at least one of the first and the second gate layers; and

reacting the metal with the at least one of the first and the second gate layers to form a silicide.

19. A method of forming a trench isolation structure on a microelectronic substrate, the method comprising the steps of:

growing a gate oxide layer on the microelectronic substrate;

depositing a polysilicon gate layer on the gate oxide layer;

depositing a nitride stop layer on the polysilicon gate layer;

etching a trench though the nitride stop layer, the polysilicon gate layer, and the gate oxide layer, the trench extending into the substrate;

filing the trench with a field oxide;

planerizing the field oxide through chemical-mechanical planarization;

removing the nitride stop layer;

recessing the planerized field oxide to a depth that is below an upper level of the polysilicon gate layer and that is at least even with an upper level of the substrate;

depositing a polysilicon adherence layer superjacent the polysilicon gate layer and the recessed field oxide;

depositing a tungsten silicide layer over the polysilicon adherence layer;

forming at least one gate structure in the tungsten silicide layer, the polysilicon adhesion layer and the polysilicon gate layer; and

forming at least one spacer adjacent the gate structure.

20. The method of claim 19 further comprising the step of:

forming an oxide on the tungsten silicide layer before performing the forming at least one gate structure step.

21. The method of claim 19, wherein the step of forming the gate structure, comprises the steps of:

patterning the tungsten silicide layer; and

etching the tungsten silicide layer and the polysilicon gate layer.

22. A microelectronic device, comprising:

a microelectronic substrate;

a gate oxide layer formed on the substrate;

a polysilicon gate layer formed on the gate oxide layer;

a trench defined through the polysilicon gate layer, the gate oxide layer and extending into the substrate; and

a field oxide in the trench, the field oxide having a field oxide level between the level of an upper surface of the substrate and the level of an upper surface of the polysilicon gate layer.

23. A microelectronic device, comprising:

a microelectronic substrate;

a gate oxide layer formed on the substrate;

a polysilicon gate layer formed on the gate oxide layer;

a trench defined through the polysilicon gate layer, the gate oxide layer and extending into the substrate;

a field oxide in the trench, the field oxide having a field oxide level between the level of an upper surface of the gate oxide and the level of an upper surface of the polysilicon gate layer;

a ploysilicon adhesion layer formed over the polysilicon gate layer and the upper surface of the field oxide.

24. The microelectronic device of claim 23, further comprising

a silicide layer formed over the polysilicon adhesion layer.

25. The microelectronic device of claim 23, further comprising

a tungsten silicide layer formed over the polysilicon adhesion layer.

26. A microelectronic device, comprising:

a microelectronic substrate having a trench formed in a surface thereof;

a field oxide in the trench, the field oxide extending from the trench, beyond the surface of the substrate;

a component formed on the field oxide, the component extending from the field oxide by a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate.

27. The microelectronic device of claim 26, further comprising an oxide spacer adjacent the component.

28. A microelectronic device, comprising:

a microelectronic substrate having a trench formed in a surface thereof;

a field oxide in the trench, the field oxide extending from the trench, beyond the surface of the substrate;

a gate structure formed on the substrate, the gate structure extending from the field oxide by a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate.

29. The microelectronic device of claim 28, further comprising an oxide spacer adjacent the gate structure.

30. A microelectronic device, comprising:

a microelectronic substrate having a recess formed in a surface thereof; and

a field oxide deposited in the trench, the field oxide extending from the trench beyond the surface of the substrate, by a height which is less than approximately one half of a height of a component formed on the field oxide.

31. The microelectronic device of claim 30, further comprising an oxide spacer adjacent the component.

32. A microelectronic device, comprising:

a microelectronic substrate having a trench formed in a surface thereof;

a gate structure formed on the substrate; and

a field oxide deposited in the trench, the field oxide extending from the trench beyond the surface of the substrate, by a height which is less than approximately one half of a height of the gate structure formed on the substrate.

33. The microelectronic device of claim 32, further comprising an oxide spacer adjacent the gate structure.

34. A microelectronic device, comprising:

a microelectronic substrate having a trench formed therein,

a field oxide within the trench and projecting therefrom by a height which is small enough to prevent the formation of spacers adjacent the field oxide pad.

METHOD AND APPARATUS FOR TRENCH ISOLATION PROCESS WITH PAD GATE AND TRENCH EDGE SPACER ELIMINATION

ABSTRACT OF THE DISCLOSURE

A microelectronic device includes a field oxide isolation pad which extends from a trench formed in a microelectronic substrate by a height which is less than approximately two times the height of a gate structure formed on the microelectronic substrate. Spacers are formed around the gate structures, although little or no spacer forms around the isolation pad. The microelectronic device is fabricated by forming a gate oxide layer on a microelectronic substrate, depositing a first gate layer on the gate oxide layer, forming a trench extending through the gate layer, the gate oxide layer and into the substrate, filling the trench with a field oxide, planarizing the field oxide, recessing the field oxide to a level above the microelectronic substrate and below an upper level of the first gate layer, forming a second gate layer over the recessed field oxide and the first gate layer, forming a conductive layer over the second gate layer, forming gate structures in the conductive layer, the first and second gate layers, and the gate oxide layer, and forming spacers adjacent the gate structures.

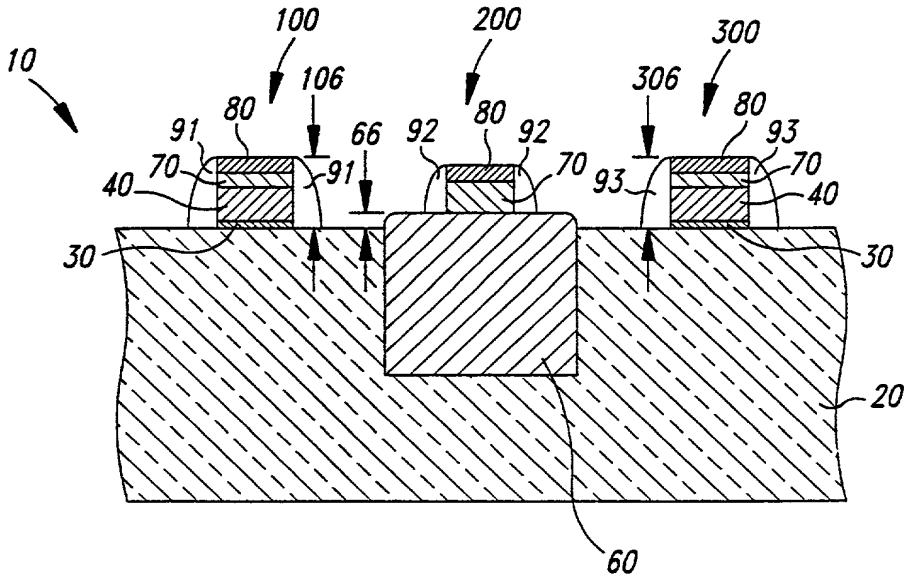

Fig. 2H

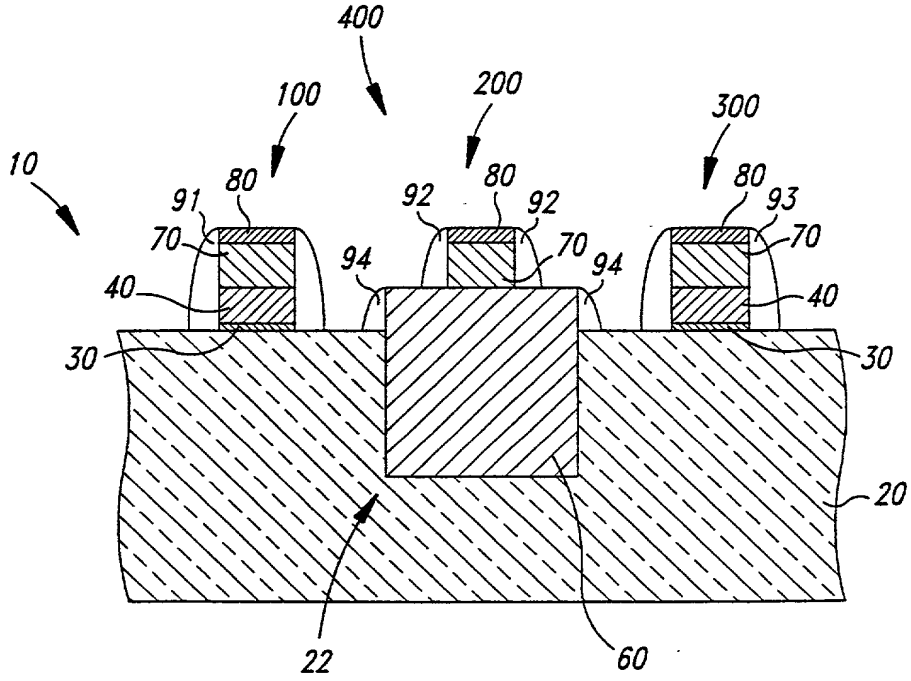

Fig. 1
(PRIOR ART)

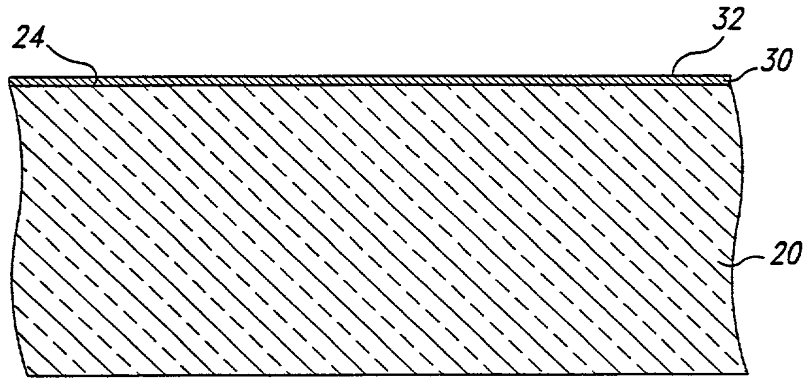

Fig. 2A

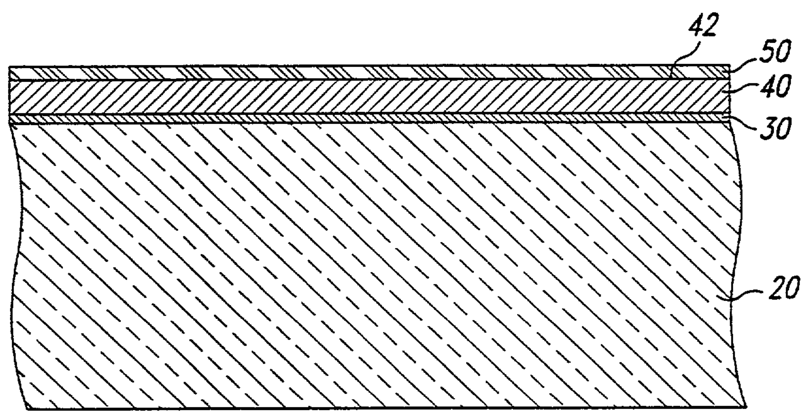

Fig. 2B

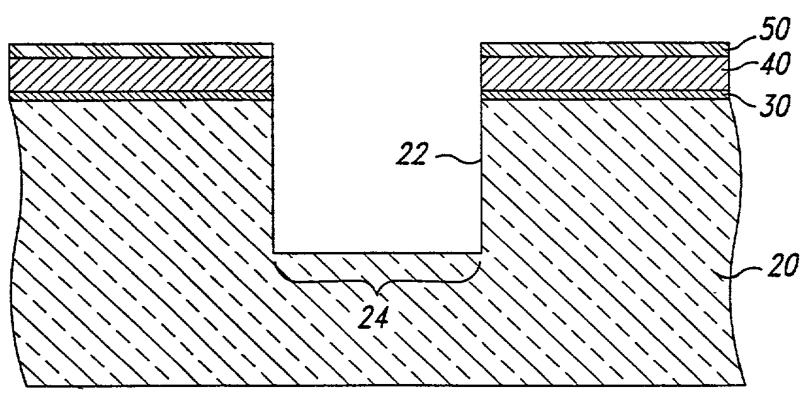

Fig. 2C

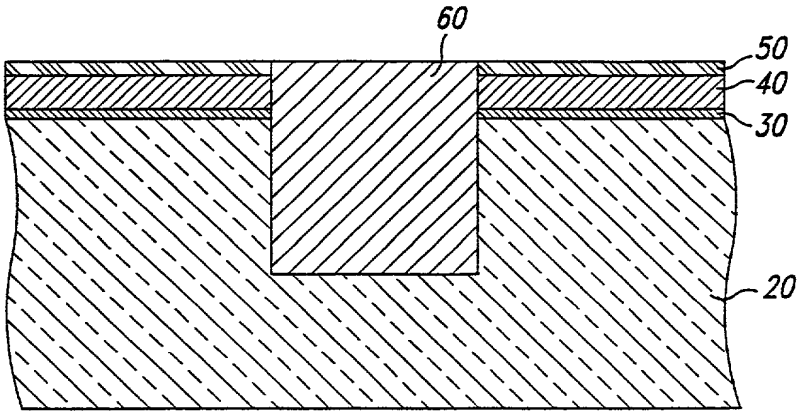

Fig. 2D

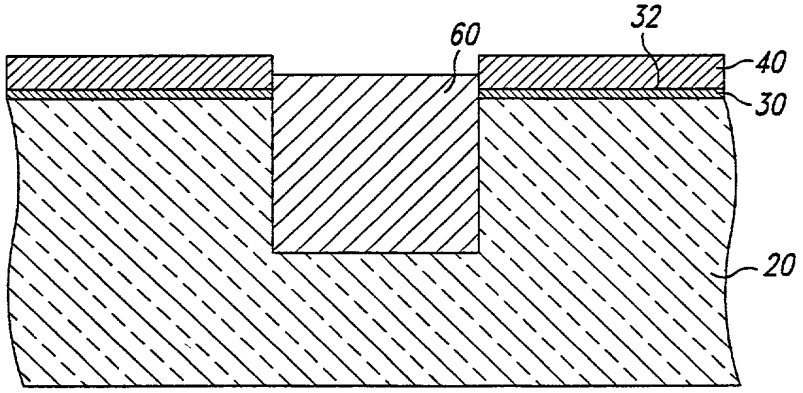

Fig. 2E

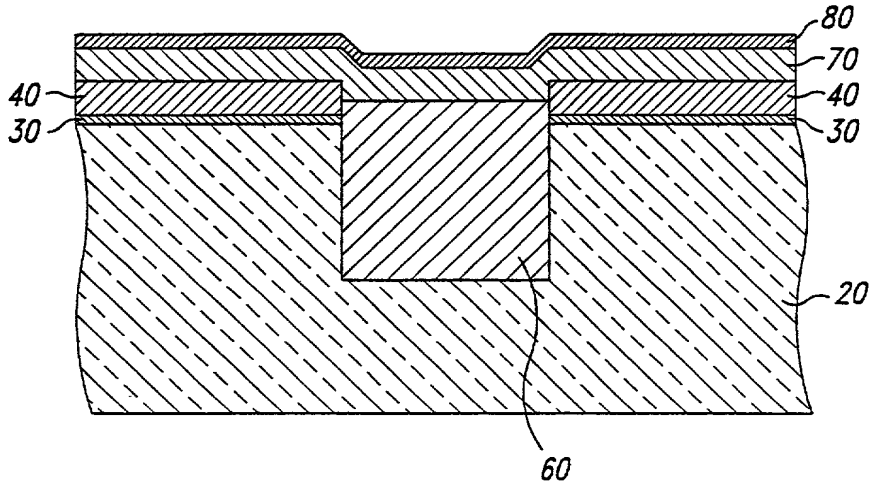
80
70
40
40
30
30
20
60

Fig. 2F

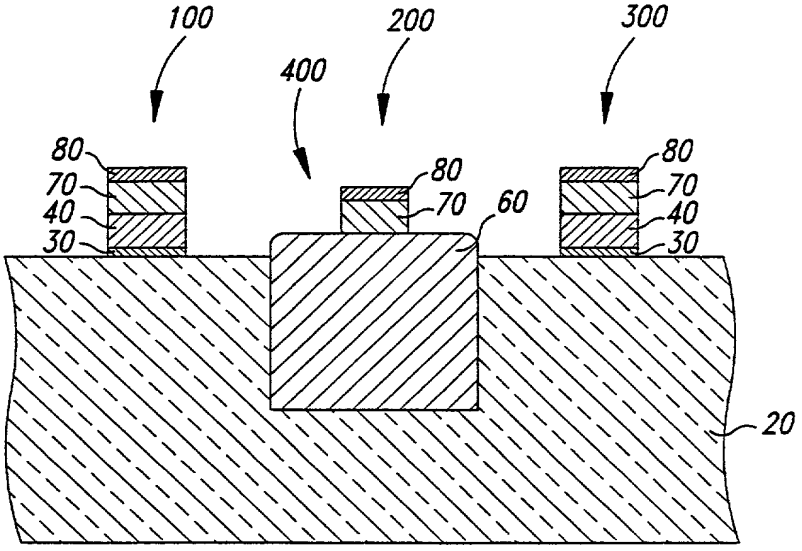
100
200
300
400
80
70
40
30
80
70
60
80
70
40
30
20

Fig. 2G

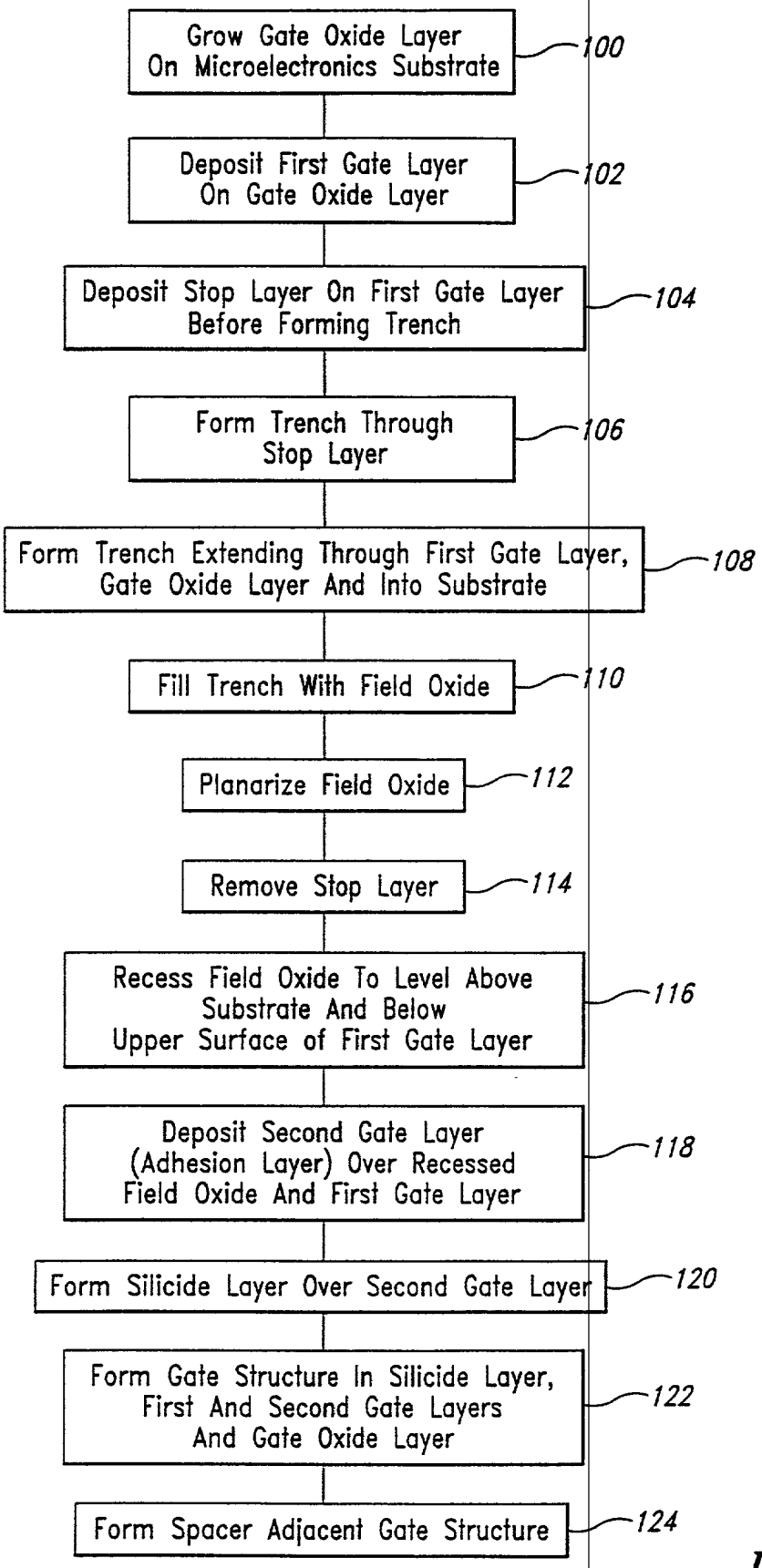
Grow Gate Oxide Layer On Microelectronics Substrate
100
Deposit First Gate Layer On Gate Oxide Layer
102
Deposit Stop Layer On First Gate Layer Before Forming Trench
104
Form Trench Through Stop Layer
106
Form Trench Extending Through First Gate Layer, Gate Oxide Layer And Into Substrate
108
Fill Trench With Field Oxide
110
Planarize Field Oxide
112
Remove Stop Layer
114
Recess Field Oxide To Level Above Substrate And Below Upper Surface of First Gate Layer
116
Deposit Second Gate Layer (Adhesion Layer) Over Recessed Field Oxide And First Gate Layer
118
Form Silicide Layer Over Second Gate Layer
120
Form Gate Structure In Silicide Layer, First And Second Gate Layers And Gate Oxide Layer
122
Form Spacer Adjacent Gate Structure
124

Fig. 3

DECLARATION

As the below-named inventors, we declare that:

Our residences, post office addresses, and citizenships are as stated below under our names.

We believe we are the original, first, and joint inventors of the invention entitled "METHOD AND APPARATUS FOR TRENCH ISOLATION PROCESS WITH PAD GATE AND TRENCH EDGE SPACER ELIMINATION," which is described and claimed in the specification and claims of Patent Application No. 09/032,231, which we filed in the United States Patent and Trademark Office on February 27, 1998 and for which a patent is sought.

We have reviewed and understand the contents of the above-entitled specification, including the claims, as amended by any amendment specifically referred to herein (if any).

We acknowledge our duty to disclose information of which we are aware which is material to patentability and examination of this application in accordance with 37 C.F.R. § 1.56(a).

We further declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that the making of willfully false statements and the like is punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and may jeopardize the validity of any patent issuing from this patent application.

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